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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/800,693 | 03/16/2004 | Shinji Ohuchi | KKH.041D2 | 1770 |

20987 7590 12/07/2006

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| EXAMINER | |
|---|---|
| KUNZER, BRIAN | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2814 | |

DATE MAILED: 12/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/800,693 | OHUCHI, SHINJI | |
| | Examiner | Art Unit | |
| | Brian Kunzer | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *12-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/497,684.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Amendments Acknowledged*

1. Applicant's amendments filed June 29th, 2006, have been received and entered. In summary claims 12, 17, 22, and 27 have been amended.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 12-15, 17-20, 22-25, and 27-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Elenius (USPN 6,441,487).

With respect to claim 12, Elenius teaches a semiconductor device (see fig. 2) comprising;

a semiconductor element (14) having a first surface and a second surface, the first surface being an opposite surface with respect to the second surface of the semiconductor element;

an electrode (18) formed at the first surface of the semiconductor element (14);

a wiring portion (30) formed on the first surface of the semiconductor element and connected to the electrode (18);

a conductive post (lower portion of 28) connected to the first surface of the semiconductor element (14) and connected to the wiring portion (30);

a resin layer (32) formed on the first surface of the semiconductor element so as to cover the first surface of the semiconductor element (14), the wiring portion (30) and a side of the conductive post (lower portion of 28);

an external connection (28) formed on the conductive post (lower portion of 28);

a protective layer (34) formed on the bottom surface (16),

wherein an end portion of the protective layer is aligned with both an end portion of the semiconductor element (14) and an end portion of the resin layer (32 or 24), and wherein the end portions (left side of fig. 2) of the protective layer (34), the semiconductor element (14), and the resin layer (32 or 24) define an outer edge (left side of fig. 2) of the semiconductor device.

With respect to claim 17, Elenius teaches a semiconductor device (see fig. 2) comprising;

a semiconductor element (14) having a first surface and a second surface, the first surface being an opposite surface with respect to the second surface of the semiconductor element;

an electrode (18) formed at the first surface of the semiconductor element (14);

a wiring portion (30) formed on the first surface of the semiconductor element and connected to the electrode (18);

a conductive post (lower portion of 28) connected to the first surface of the semiconductor element (14) and connected to the wiring portion (30);

a resin layer (32) formed on the first surface of the semiconductor element so as to cover the first surface of the semiconductor element (14), the wiring portion (30) and a side of the conductive post (lower portion of 28);

an external connection (28) formed on the conductive post (lower portion of 28);

a protective layer (34) formed on the bottom surface (16), wherein an end portion of the protective layer is aligned with both an end portion of the semiconductor element (14) and an end portion of the resin layer (32 or 24);

***a side surface*** of the semiconductor element (14) being exposed from the resin layer (24) and the protective layer (34), and wherein all three layers are aligned, and wherein the end portions (left side of fig. 2) of the protective layer (34) and the resin layer (32 or 24), and the exposed side surface of the semiconductor element (14), define an outer edge (left side of fig. 2) of the semiconductor device.

With respect to claim 22, Elenius teaches a semiconductor device (see fig. 2) comprising;

a semiconductor element (14) having a first surface and a second surface, the first surface being an opposite surface with respect to the second surface of the semiconductor element;

an electrode (18) formed at the first surface of the semiconductor element (14);

a wiring portion (30) formed on the first surface of the semiconductor element and connected to the electrode (18);

a conductive post (lower portion of 28) connected to the first surface of the semiconductor element (14) and connected to the wiring portion (30);

a resin layer (32) formed on the first surface of the semiconductor element so as to cover the first surface of the semiconductor element (14), the wiring portion (30) and a side of the conductive post (lower portion of 28);

an external connection (28) formed on the conductive post (lower portion of 28);

a protective layer (34) formed on the bottom surface (16), wherein an end portion of the protective layer is aligned with both an end portion of the semiconductor element (14) and an end portion of the resin layer (32 or 24);

***only*** a side surface of the semiconductor element (14) being exposed from the resin layer (24) and the protective layer (34), and wherein an end portion of the protective layer is aligned with both the side surface of the semiconductor element and an end portion of the resin layer, and wherein the end portions (left side of fig. 2) of the protective layer (34) and the resin layer (32 or 24), and the side surface of the semiconductor element (14), define an outer edge (left side of fig. 2) of the semiconductor device.

With respect to claim 27, Elenius teaches a semiconductor device (see fig. 2) comprising;

a semiconductor element (14) having a first surface and a second surface, the first surface being an opposite surface with respect to the second surface of the semiconductor element;

an electrode (18) formed at the first surface of the semiconductor element (14);

a wiring portion (30) formed on the first surface of the semiconductor element and connected to the electrode (18);

a conductive post (lower portion of 28) connected to the first surface of the semiconductor element (14) and connected to the wiring portion (30);

a resin layer (32) formed on the first surface of the semiconductor element so as to cover the first surface of the semiconductor element (14), the wiring portion (30) and a side of the conductive post (lower portion of 28);

an external connection (28) formed on the conductive post (lower portion of 28);

a protective layer (34) formed on the bottom surface (16), wherein an end portion of the protective layer is aligned with both an end portion of the semiconductor element (14) and an end portion of the resin layer (32 or 24);

a protective layer (34) formed on the second surface of the semiconductor element (14), wherein a side surface of the protective layer is in a same plane with both a side surface of the semiconductor element and a side surface of the resin layer, and wherein the side surfaces (left side of fig. 2) of the protective layer (34), the semiconductor element (14), and the resin layer (32 or 24) define an outer edge (left side of fig. 2) of the semiconductor device.

With respect to claims 13, 18, 23, and 28 – all claims having similar subject matter - Elenius teaches the use of polyimide, a synthetic resin, as a passivation layer. (column 7, line 46)

With respect to claims 14, 19, 24, and 29 – all claims having similar subject matter - Elenius teaches the use of organic compounds or epoxy substances in the protective layer (column 8, lines 28-31).

With respect to claims 15, 20, 25, and 30 – all claims having similar subject matter - Elenius teaches the use of solder balls as external connections (column 6, line 63).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 16, 21, 26, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Elenius-487 as applied to claims 12, 17, 22, and 27 above, and further in view of Kim-867.

With respect to claims 16, 21, 26, and 31 – all claims having similar subject matter – Elenius teaches all that is stated above and, from fig. 2, the use of a conductive solder post (lower portion of 28) attached to a semiconductor layer (14) through a wiring portion (30) at its base, including a solder ball (28) connected to the top of the post.

Elenius does not teach the use of copper in the conductive post.

However, Kim, drawn to semiconductor devices, teaches the use of copper as a connection post (123 and 124) between a solder ball (130) and a wiring portion (122) that runs to the semiconductor element (110). (see fig. 1 and column 4, lines 13-16)

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to replace the conductive material in the post of Elenius with the copper as described

by Kim because the use of copper as an electrical connector is well known in the art due to its reliability, availability, and inexpensiveness.

***Response to Arguments***

4. Applicant's arguments filed June 29th, 2006 have been fully considered but they are not persuasive.

Applicant makes the following arguments with respect to independent claims 12, 17, 22, and 27:

> As relied upon by the Examiner, Fig. 2 of the Elenius et al. reference includes a second passivation layer 32 formed at front surface 12 of semiconductor wafer 14, and protective coating 34 formed at a rear surface 16 of semiconductor wafer 14. However, as described in column 5, lines 48-50 of the Elenius et al. reference, Fig. 2 is a cross-sectional view of a portion of a semiconductor wafer used to form the chip scale packaged integrated circuit shown in Fig. 1.
>
> Accordingly, Fig. 2 of the Elenius et al. reference merely shows a part or portion of the chip scale packaged integrated circuit of Fig. 1. That is, Fig. 2 is merely a cross-sectional view, and does not show the whole area of the chip scale packaged integrated circuit of Fig. 1 of the Elenius et al. reference. In Fig. 1 of the Elenius et al. reference, the outer perimeter of the chip scale packaged integrated circuit 8 is illustrated by reference numeral 21. However, Fig. 2 of the Elenius et al. reference does not specifically show any portion corresponding to the outer perimeter 21 shown in Fig. 1. There is no description in the Elenius et al. reference that the end portions shown in Fig. 2 corresponds to outer perimeter 21 of Fig. 1. Accordingly, the Elenius et al. reference does not specifically show or disclose end portions of a protective layer, a semiconductor element and a resin layer that define an outer edge of a semiconductor device, as would be necessary to meet the features of claim 12. Applicant therefore respectfully submits that the semiconductor device of claim 12 distinguishes over the Elenius et al. reference as relied upon by the Examiner.

In response to this argument, Examiner contends that while fig. 2 may in fact be a cross-sectional portion of the device shown in fig. 1, fig. 2 shows the portion of fig. 1 extending from the bump contacts (28) and past the semiconductor electrodes (18) to the outer perimeter (21).

This is clearly evidenced by the fact that the electrodes (18) are placed along the outer perimeter (21) of the device (8) shown in fig. 1, and fig. 2 clearly shows this detail out to the perimeter (21). Accordingly, one of ordinary skill in the art would recognize that the left hand side surface of fig. 2 corresponds to the end portions (perimeter 21) of the device shown in fig. 1.

5. Furthermore, Applicant's attention is directed to column 8, lines 20-41 and column 9, lines 42-50 of Elenius et al., wherein not only is it explicitly stated, "the final dimensions of protective coating (34) are the same as the final dimensions of the die [i.e. 14]," but describe the step of dicing through all the layers (resin layers, semiconductor element, protective layer, ... etc.) of the package (after they have been deposited). This dicing process inherently creates an aligned side surface for all the packaging layers, defining the outer edge of the package, and thus, meeting the limitations disclosed in the disputed independent claims 12, 17, 22, and 27.

***Conclusion***

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Kunzer whose telephone number is (571) 272-5054. The examiner can normally be reached on Monday-Friday 8:00-4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BK
11/29/06

ANH D. MAI
PRIMARY EXAMINER